A memory device having multiple interfaces enables use of a proprietary interface during device operation while allowing programming of the device through a programming interface that may be released to motherboard manufacturers. Having separate interfaces allows a memory device manufacturer to withhold a device interface specification from tool enabling customers such as BIOS programmers.

Please replace the paragraph beginning at page 12, line 20 and ending at page 13, line 7 with the following:

Figure 6 illustrates one embodiment of interface selection circuitry. Memory device 650 includes selection circuitry coupled to the pads of the device for switching between multiple device interfaces. In one embodiment, the selection circuitry coupled to pad 609, for example, includes control multiplexer 680 and drivers 684, 686, and 688. In one embodiment, drivers 684, 686, and 688 may be coupled to different control function circuitry within memory device 650. For example, driver 686 may be coupled to chip enable circuitry 687 used during testing; driver 688 may be coupled to row / column address selection circuitry 689 to toggle between a low and high order address during programming; and driver 684 may be coupled to clock circuitry 685 used during in-system device operations. Two configuration lines 639 and 602 are coupled to control multiplexer 680 and used to select between the multiple interfaces containing the different device functions.

IN THE CLAIMS

Please cancel claims 1-20 without prejudice.

Please add the following new claims:

Rule 1.126

19.

~~21.~~ (New) A memory device, comprising a plurality of different interfaces to operate the memory device in a plurality of different modes.

Rule 1.126

20.

~~22.~~ (New) The memory device of claim ~~21~~ 19, further comprising a configuration device to select among the plurality of different interfaces.

Rule 1.126

21.

~~23.~~ (New) The memory device of claim ~~22~~ 20, wherein the plurality of different interfaces comprises:

a test interface to test the memory device for defects;

a programming interface to program the memory device with a code; and

an operation interface to operate the memory device in an operation mode.

Rule 1.126

22.

~~24.~~ (New) The memory device of claim ~~23~~ 21, wherein the memory device is a flash memory and the test interface is a standard flash memory interface.

Rule 1.126

23.

~~25.~~ (New) The memory device of claim ~~23~~ 21, wherein the operation interface is a proprietary interface.

Rule 1.126

24.

~~26.~~ (New) The memory device of claim ~~22~~ 20, wherein the configuration device comprises:

a plurality of drivers, each of the plurality of drivers coupled between a device pad and a device circuit, each of the plurality of drivers having a control input; and

a multiplexer coupled to the control input of each of the plurality of drivers to select one of the plurality of drivers.

Rule 1.126
25.

~~27.~~ (New) The memory device of claim ~~26~~ 24, wherein the plurality of different interfaces comprises:

a test interface to test the memory device for defects;

a programming interface to program the memory device with a code; and

an operation interface to operate the memory device in an operation mode.

Rule 1.126
26.

~~28.~~ (New) A component board, comprising:

a processor; and

a memory device coupled with the processor, the memory device comprising a plurality of different interfaces to operate the memory device in a plurality of different modes.

Rule 1.126
27.

~~29.~~ (New) The component board of claim ~~28~~ 26, further comprising a configuration device to select among the plurality of different interfaces.

Rule 1.126
28.

~~30.~~ (New) The component board of claim ~~29~~ 27, wherein the configuration device comprises:

a plurality of drivers, each of the plurality of drivers coupled between a device pad and a device circuit, each of the plurality of drivers having a control input; and

a multiplexer coupled to the control input of each of the plurality of drivers to select one of the plurality of drivers.

Rule 1.126

29.

~~31.~~ (New) The component board of claim ~~30~~ 28, wherein the plurality of different interfaces comprises:

a test interface to test the memory device for defects;

a programming interface to program the memory device with a code; and

an operation interface to operate the memory device in an operation mode.

Rule 1.126

30.

~~32.~~ (New) The component board of claim ~~31~~ 29, wherein the memory device is a flash memory, the test interface is a standard flash memory interface, and the operation interface is a proprietary interface.

Rule 1.126

31.

~~33.~~ (New) The component board of claim ~~29~~ 27, wherein the memory device is a BIOS memory.

Rule 1.126

32.

~~34.~~ (New) A computer system, comprising:

a peripheral device; and

a system board coupled to the peripheral device, the system board comprising:

a processor; and

a memory device coupled with the processor, the memory device comprising a plurality of different interfaces to operate the memory device in a plurality of different modes.

Rule 1.126

33.

~~35.~~ (New) The computer system of claim ~~34~~ 32, further comprising a configuration device to select among the plurality of different interfaces.